Electronic Version
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Claims

[c1] 1. A source driver for driving sources of a plurality of thin film transistors, the source driver comprising:
a shift register, for receiving digital image data;
a latch, coupled to the shift register, for receiving digital image data from the shift register;
a level shifter, coupled to the latch, for receiving digital image data from the latch and for shifting a voltage level of digital image data; and
an analog circuit, coupled to the level shifter, for receiving the digital image data, converting the digital image data to a corresponding analog image data, and outputting the analog image data to the plurality of sources;
wherein a power supply voltage level and a ground voltage level are provided to the level shifter and the analog circuit; at least one middle voltage level between the power supply voltage level and the ground voltage level is provided to the level shifter and the analog circuit.

[c2] 2.The source driver of claim 1, wherein each of the level shifter and the analog circuit has a positive polarity and a negative polarity; the power supply voltage level and the middle voltage level are provided to the level shifter

with the positive polarity and the analog circuit with the positive polarity; the middle voltage level and the ground level are provided to the level shifter with the negative polarity and the analog circuit with the negative polarity.

[c3] 3.The source driver of claim 1, wherein when there are two or more middle voltage levels are provided, the middle voltage level provided to the level shifter with the positive polarity and the analog circuit with the positive polarity is larger than the ground level and equal to or less than a half of the power supply voltage level, and the middle voltage level provided to the level shifter with the negative polarity and the analog circuit with the negative polarity is larger than or equal to a half of the power supply voltage level and is smaller than the power supply voltage level.

[c4] 4. The source driver of claim 1, wherein the latch further comprises a first level latch and a second level latch, wherein the first level latch sequentially receives digital image data, and
digital image data comprises image data of horizontal lines, and the horizontal lines are sequentially arranged, when the first latch completely receives image data of one horizontal line, the first latch outputs image data of the one horizontal line to the second level latch, and continues receiving image data of next horizontal line,

the second level latch outputs the image data of the one horizontal line to the level shifter.

[c5] 5.The source driver of claim 1, wherein the analog circuit with the positive polarity comprises a digital-to-analog converter with the positive polarity and an output buffer with the positive polarity.

[c6] 6.The source driver of claim 5, wherein the digital-to-analog converter with the positive polarity provides an image data conversion with the positive polarity.

[c7] 7. The source driver of claim 5, wherein the output buffer with the positive polarity is a unit-gain and negative-feedback operational amplifier.

[c8] 8.The source driver of claim 1, wherein the analog circuit with the negative polarity comprises a digital-to-analog converter with the negative polarity and an output buffer with the negative polarity.

[c9] 9.The source driver of claim 8, wherein the digital-to-analog converter with the negative polarity provides an image data conversion with the negative polarity.

[c10] 10. The source driver of claim 8, wherein the output buffer with the negative polarity is a unit-gain and negative-feedback operational amplifier.

[c11] 11. A source driver for a plurality of sources of a plurality of thin film transistors, comprising:
an analog circuit with a positive polarity, coupled to a power supply voltage level and a first middle voltage level, receiving a gamma voltage and digital image data, converting digital image data to corresponding analog image data, and outputting analog image data to the sources;
an analog circuit with a negative polarity, coupled to a ground level and a second middle voltage level, receiving a gamma voltage and digital image data, converting digital image data to corresponding analog image data, and outputting analog image data to the sources;
a first level shifter, coupled to the power supply voltage level and the first middle voltage level, receiving input data, converting a voltage level of digital image data, and outputting the voltage level of digital image data to the analog circuit with the analog circuit with the positive polarity; and
a second level shifter, coupled to the ground level and the second middle voltage level, receiving input data, converting a voltage level of digital image data, and outputting the voltage level of digital image data to the analog circuit with the analog circuit with the negative polarity.

[c12] 12.The source driver of claim 11, wherein when the first middle voltage level is the same as the second middle voltage level, the first middle voltage level is a half of the power supply voltage level and the second middle voltage level is a half of the power supply voltage level.

[c13] 13. The source driver of claim 11, wherein when the first middle voltage level and the second middle voltage level are not equal, the first middle voltage level is larger than the ground level and smaller than or equal to a half of the power supply voltage level, and the second middle voltage level is larger than or equal to a half of the power supply voltage level and is smaller than the power supply voltage level.

[c14] 14.The source driver of claim 11, wherein the analog circuit with the positive polarity comprises a digital-to-analog converter and an output buffer.

[c15] 15.The source driver of claim 14, wherein the output buffer is an output buffer with the positive polarity comprising a unit-gain and negative-feedback operational amplifier.

[c16] 16. The source driver of claim 11, wherein the analog circuit with the negative polarity comprises a digital-to-analog converter and an output buffer.

[c17] 17.The source driver of claim 16, wherein the output buffer is an output buffer with the negative polarity comprising a unit-gain and negative-feedback operational amplifier.

[c18] 18.A liquid crystal display, comprising:
a plurality of thin film transistors, each of the thin film transistors having a gate, a source, and a drain;
a gate driver circuit, coupled to the gates of the thin film transistors, for outputting a signal to selectively turn on the thin film transistors; and
a source driver circuit, coupled to the sources of the thin film transistors, the source driver circuit comprising:
an analog circuit with a positive polarity, coupled to a power supply voltage level and a first middle voltage level, receiving a gamma voltage and digital image data, converting digital image data to corresponding analog image data, and outputting analog image data to the sources;
an analog circuit with a negative polarity, coupled to a ground level and a second middle voltage level, receiving a gamma voltage and digital image data, converting digital image data to corresponding analog image data, and outputting analog image data to the sources;
a first level shifter, coupled to the power supply voltage level and the first middle voltage level, receiving input

data, converting a voltage level of digital image data, and outputting the voltage level of digital image data to the analog circuit with the analog circuit with the positive polarity; and

a second level shifter, coupled to the ground level and the second middle voltage level, receiving input data, converting a voltage level of digital image data, and outputting the voltage level of digital image data to the analog circuit with the analog circuit with the negative polarity.

[c19] 19. The liquid crystal display of claim 18, wherein when the first middle voltage level is the same as the second middle voltage level, the first middle voltage level is a half of the power supply voltage level and the second middle voltage level is a half of the power supply voltage level.

[c20] 20.The liquid crystal display of claim 18, wherein when the first middle voltage level is not the same as the second middle voltage level, the first middle voltage level is larger than the ground level and smaller than or equal to a half of the power supply voltage level, and the second middle voltage level is larger than or equal to a half of the power supply voltage level and is smaller than the power supply voltage level.

[c21] 21.The liquid crystal display of claim 18, wherein the analog circuit with the positive polarity comprises a digital-to-analog converter and an output buffer.

[c22] 22.The liquid crystal display of claim 21, wherein the output buffer is an output buffer with the positive polarity comprising a unit-gain and negative-feedback operational amplifier.

[c23] 23. The liquid crystal display of claim 18, wherein the analog circuit with the negative polarity comprises a digital-to-analog converter and an output buffer.

[c24] 24.The liquid crystal display of claim 23, wherein the output buffer is an output buffer with the negative polarity comprising a unit-gain and negative-feedback operational amplifier.